UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,799	06/27/2003	Ken Drottar	42P16616	6507

8791 7590 01/24/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
NGUYEN, KHANH V	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,799	DROTTAR, KEN	
	Examiner	Art Unit	
	Khanh V. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,14-19,22-27 and 57-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14-19,22-27 and 57-68* is/are rejected.

7)☒ Claim(s) *12,13,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings (Figures 3 and 4) are objected to because they are unreadable. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 4, 5 are objected to because of the following informalities:

Claim 4, page 3, line 6, "first" should correctly be –second--.

Claim 5 page 4, line 2, "first" should correctly be –second--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim15, it is not clear what is meant by "precharge artifacts". The specification needs to be more descriptive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 9-11, 14, 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Patterson III (4,446,444).

Regarding claims 1, 16, Patterson III (Fig. 4) discloses a CMOS amplifier comprising: an amplifier (N1, P2; N4, P4); a first inverter (P5, N5) having an input (gate) coupled to an output (drain) of the amplifier (P4, N4); and transistors (P6, N6) operable as a second inverter having an input (gate) coupled to an output (drain) of the first inverter and an output (drain of transistors (P6, N6)), wherein the output (drain) of the second inverter (P6, N6) is fed back (FB) to an input (INV INPUT) of the amplifier.

Regarding claim 16, wherein the first and second inverters, and the amplifier can be read as a delay and gain circuit.

Regarding claim 2, wherein the amplifier (N1, P2; N4, P4) is a CMOS amplifier.

Regarding claim 3 wherein the CMOS amplifier of Patterson III can be implemented as a hybrid Bazes and Chappell amplifier.

Regarding claims 9, 10, 17, 18 wherein the output (drain/OUTPUT) of the second inverter (P6, N6) is fed back (FB) to an input (INV INPUT) of the amplifier as a negative/positive feedback.

Regarding claims 11, 19, wherein the amplifier provides positive feedback and the output of the second inverter is fed back to the amplifier as negative feedback.

Regarding claim 14, wherein the output (OUTPUT) is coupled to the output of the second inverter.

Claims 1-4, 9-11, 14, 16-19, 22, 25, 57, 60, 63, 66 are rejected under 35 U.S.C. 102(b) as being anticipated by Hu (5,990,708).

Regarding claims 1, 16, Hu (Fig. 2) discloses a differential input buffer comprising: an amplifier (50, 52, 56, 58, 62, 64); a first inverter (76, 78) having an input (gate) coupled to an output (N2) of the amplifier (50, 52, 56, 58, 62, 64); and a second inverter (80, 82) having an input (gate) coupled to an output (drain/N7) of the first inverter (76, 78) and an output (drain/N8), wherein the output (drain/N8) of the second inverter (80, 82) is fed back to an input of the amplifier (50, 52, 56, 58, 62, 64) at node

(N1) via transistors (74, 66). Regarding claim 16, wherein the first and second inverters, and the amplifier can be read as a delay and gain circuit.

Regarding claim 2, wherein the amplifier (50, 52, 56, 58, 62, 64) is a CMOS amplifier.

Regarding claim 3 wherein the CMOS amplifier of Hu operable as a hybrid Bazes and Chappell amplifier.

Regarding claims 4, 57, 63, wherein, the amplifier (50, 52, 56, 58, 62, 64) includes a first (62), a second (56) and a third pMOS (50) transistor and a first (64), a second (58) and a third nMOS (52) transistor; a gate of the first pMOS transistor (62) and a gate of the first nMOS transistor (64) are coupled to an input (VREF); a gate of the second pMOS transistor (56) and a gate of the **second** nMOS transistor (58) are coupled to a drain (N1) of the first pMOS transistor (62) and a drain of the first nMOS transistor (64); and a gate of the third pMOS transistor (50) and a gate of the third nMOS transistor (52) are coupled to an input (IN) which can be read as an inverse input.

Regarding claims 9, 10, 17, 18 wherein the output (N8) of second inverter (80, 82) is fed back to an input of the amplifier (50, 52, 56, 58, 62, 64) at node (N1) via transistors (74, 66) as a negative/positive feedback.

Regarding claims 11, 19, wherein the amplifier provides positive feedback and the output of the second inverter is fed back to the amplifier as negative feedback.

Regarding claim 14, wherein the output (OUT) is coupled to the output of the second inverter.

Regarding claim 22, Hu (Fig. 2) discloses a differential buffer comprising: an input; an inverse input; an output; a first pMOS transistor (62) having a gate coupled to the VREF, which can be read as the input of the amplifier; a second pMOS transistor (56); a third pMOS transistor (50) having a gate coupled to the input (IN), which can be read as an inverse input of the amplifier and having a source coupled to a source of the first pMOS transistor (62) and to a drain of the second pMOS transistor (56); a first nMOS transistor (64) having a gate coupled to the input (VREF) of the amplifier; a second nMOS transistor (58) having a gate coupled to a drain of the first pMOS transistor (64), a drain of the first nMOS transistor (64), and to a gate of the second pMOS transistor (56); and a third nMOS transistor (52) having a gate coupled to the inverse input (IN) of the amplifier, a drain coupled to a drain of the third pMOS transistor (50) and a source coupled to a source of the first nMOS transistor (64) and to a drain of the second nMOS transistor (58), wherein the output (N2) of the amplifier is coupled to the drain of the third pMOS transistor (50) and to the drain of the third nMOS transistor (52).

Regarding claims 25, 60, 66, further comprising a control input (N1 of Hu), wherein the gate of the second nMOS transistor and the gate of the second pMOS transistor are coupled to the control input.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-8, 23, 24, 26, 27, 58, 59, 61, 62, 64, 65, 67, 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu in view of Greason et al. (5,939,942).

Regarding claims 5, 23, 58, 64, Hu discloses the claimed invention except a resistor having the connection as claimed.

Greason et al. (Fig. 6) disclose a differential input buffer comprises resistor (621) having a connection as claimed.

Hu and Greason et al. are analogous art because they are from the same field of endeavor, namely buffer. Accordingly, it would have been obvious in view of the reference, taken as a whole, to have modified the circuit of Hu to have included a resistor between the gate of transistors (56, 58) and the drain of transistors (62, 64), as taught by Greason et al. Such a modification would have imparted the advantageous benefit of provided the bias voltage at common gate of transistors (56, 58) to be different from the output, as taught by Greason et al., see column 5, lines 5-10, to Hu reference, thereby suggesting the obviousness of such a modification.

Regarding claims 6-8, the differences between the claims and Hu/Patterson III is the size of the inverters. However optimizing the size of an inverter for a given intended use would be a matter of routine experimentation and thus would have been obvious to one of ordinary skill in the art to change the size of transistors (76, 78, 80, 82) as desired to obtain optimum operating parameters.

Regarding claims 24, 59, 65, Greason et al. together with Hu disclose the claimed invention except the size of the resistor as claimed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented the specific values of the components, since they are based on the routine experimentation to obtain the optimum operating parameters.

Regarding claim 26, 27, 61, 62, 67, 68, the differences between the claims and Hu/Patterson III is the size of the transistors claimed. However optimizing the size of the transistors for a given intended use would be a matter of routine experimentation and thus would have been obvious to one of ordinary skill in the art to change the size of transistors as desired to obtain optimum operating parameters.

Allowable Subject Matter

Claims 12, 13, 20, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 12, 13, 20, 21 call for, among others, the amplifier mixes the positive feedback and the negative feedback and the resistor is included in a circuit that mixes positive feedback provided by the amplifier and negative feedback provided to the amplifier from the output of the second inverter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh V. Nguyen whose telephone number is (571) 272-1767. The examiner can normally be reached from 8:00 AM - 3:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KHANH V. NGUYEN
PRIMARY EXAMINER